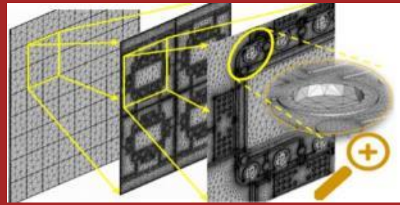
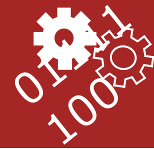


Multiscale Multiphysics Simulation of Power Integrated devices, Challenges and Opportunities

Marius Purcar
Facultatea de Inginerie Electrica
Dep. de Electrotehnica si Masurari

iDev40 - Integrated Development 4.0



iDev40 - Integrated Development 4.0 > **Consortium**

• Austria • Germany • Italy • Belgium • Spain • Romania

H2020-ECSEL-2017-1-IA-two-stage

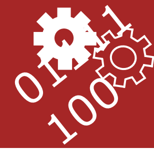
6/1.1.3 H/26.11.2019, MYSMIS 122386

Consortium

The consortium includes market leaders in their domain, small- and medium sized companies, research institutes and universities, having excellent manufacturing and science background. All project partners are fully committed to achieve the very challenging project goals.

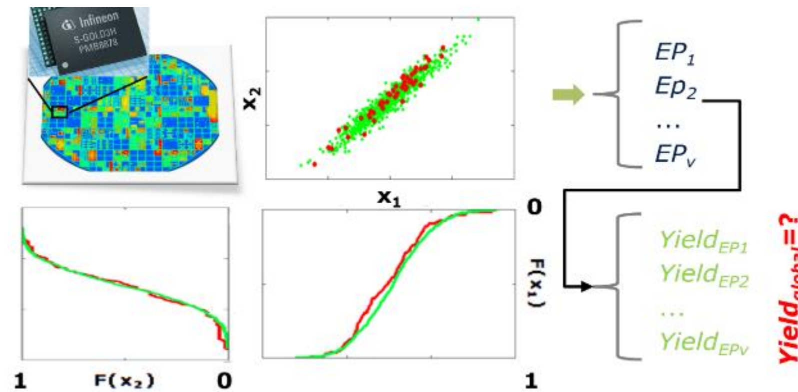
The strategic goal of the iDev40 project is to enhance essential competencies for Electronic Components and Systems "Made in Europe" to sustainably support European companies that have dominant global positions in key application areas

UTCN Role within iDev40

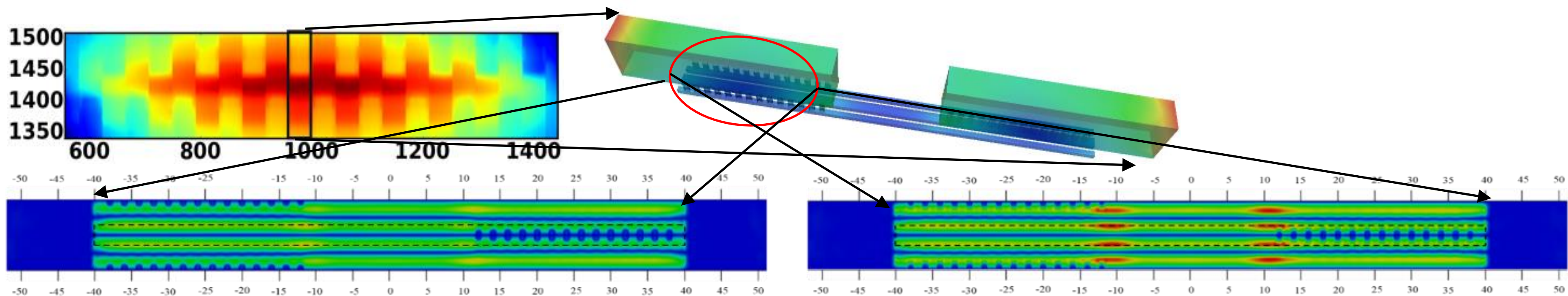


Objective 7.2 activities of Infineon Technologies Romania and Technical University Cluj-Napoca linked to WP2 task T2.4.1. Design methodology development focused on:

- Yield estimation flows → extension of the distribution modelling together with other statistical approaches to estimate the yield considering also the correlations between test parameters.



- Reliability analysis → efficient modelling of electro-thermo-mechanical stress during fast power cycling operation of power integrated circuits (PIC) in order to correctly predict the failure position and enable relative reliability comparison between design variants.



UTCN Project Team

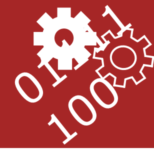
- Yield estimation flows

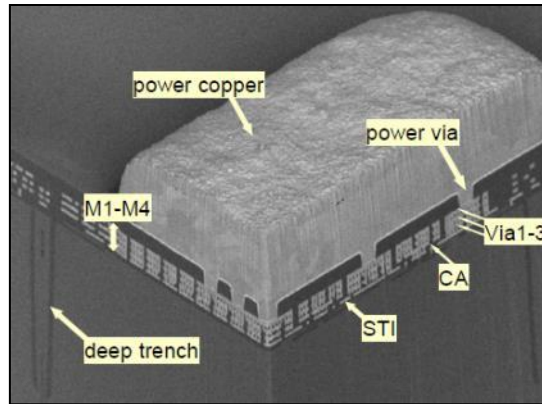
Carbunescu- Stoenescu	Bianca-Raluca
Grumeza	Andrei
Kovacs Lupou	Ingrid Maria
Neag	Marius Gheorghe
Onet	Raul Ciprian
Plesa	Cosmin Sorin
Rusu	Alecsandra
Topa	Mariana Dana

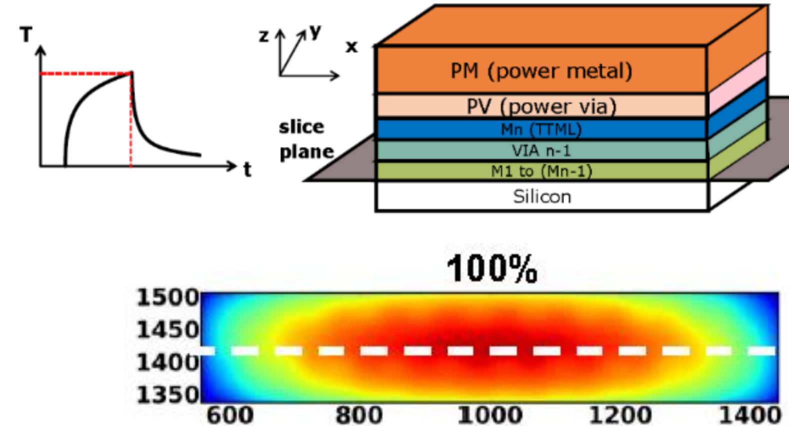
- Reliability analysis

Florea	Ciprian Ionut
Bojita	Ioan Adrian
Dobre	Luiza Adriana
Munteanu	Calin
Pacurar	Claudia
Topa	Vasile
Purcar	Ioan Marius

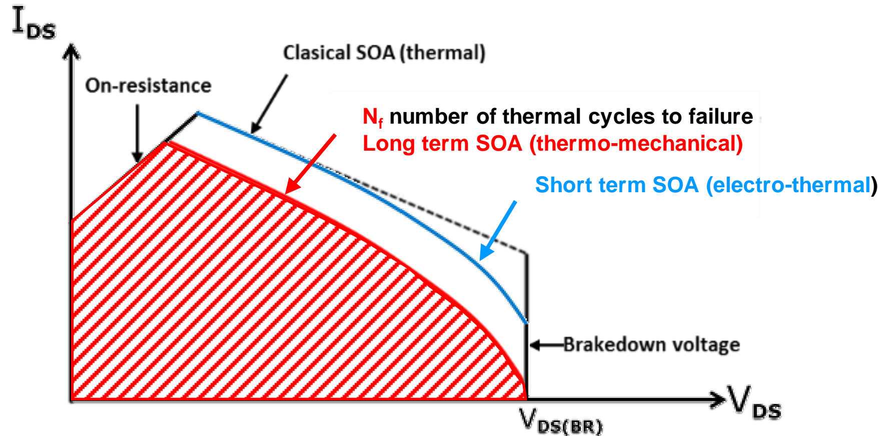
Safe – Operating Area (SOA) of Power Integrated Circuits







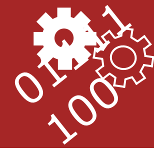
- **For DMOS devices SOA is limited to:**



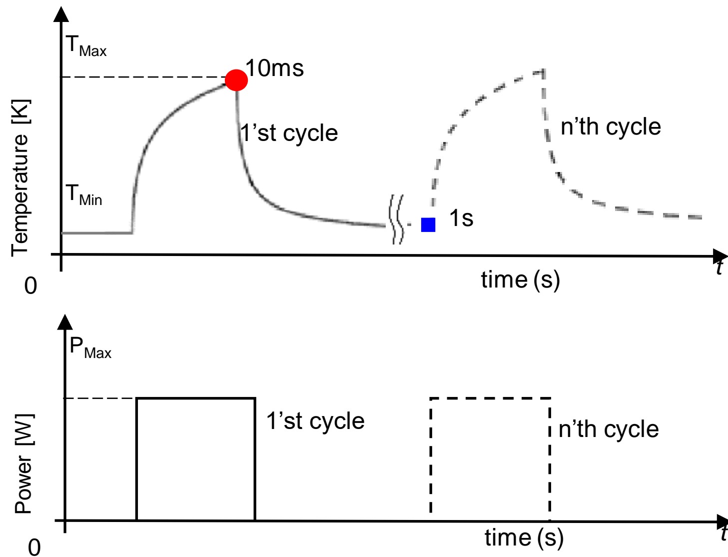
- Short term due to electro-thermal effects
- Long term due to device degradation after several heating – cooling repetitive cycles

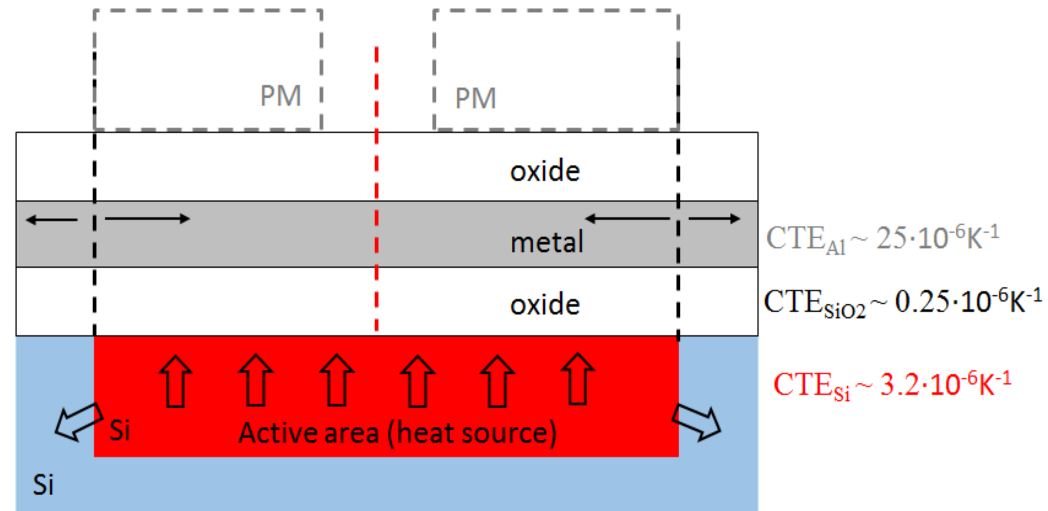
Source: PhD Simon Dan “Reliability Improvement of DMOS Power Switches Which Operate Under Repetitive Thermal Cycling”

Thermal Cycling Effects in PIC

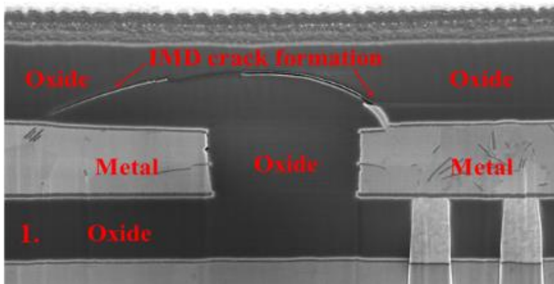


- **Temperature distribution inside the device operating under a power pulse:**

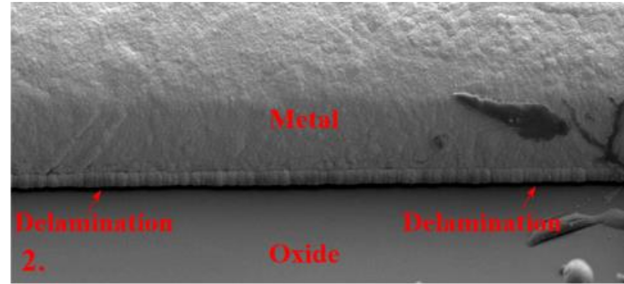




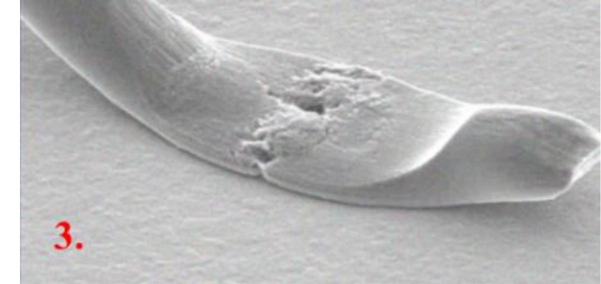
Different thermal expansion coefficient (CTE) → Different deformation of materials → Accumulate mechanical stress with each cycle → Failure mechanisms which limit the long-term SOA:



Inter-metal dielectric (IMD) cracking



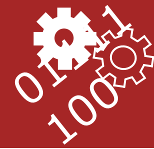
Metal delamination from dielectric oxide layer



Bond-wire degradation

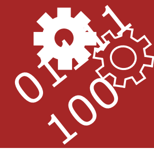
Sources:
[1] and [2] PhD Simon Dan "Reliability Improvement of DMOS Power Switches Which Operate Under Repetitive Thermal Cycling"
[3] R. Pufall "Wire Bonding Degradation Induced By Temperature Gradients Under Active Cyclic Loading"

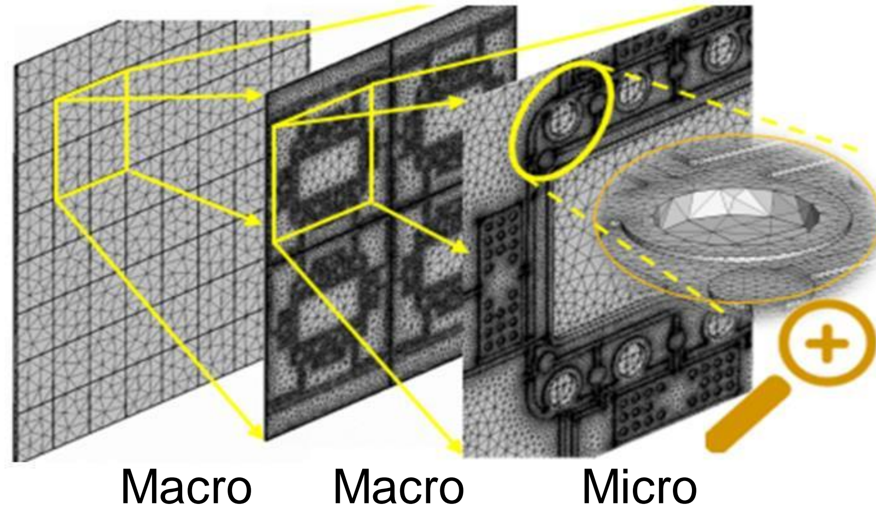
Multiscale-Multigrid Simulator of Electro-Thermo-Mechanical Processes in IC's



- Iterative simulation by progressively increased resolution

Simulation Strategy - Work Flow
Chip Level Thermo-Mechanical Simulation





Macro Macro Micro

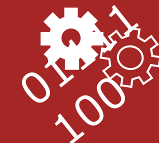
3D CIP model CADENCE + Salome-Meca (SM)	→	**SET4CIP** Optimal mesh generation scripts on top of SM+NETGEN (GMESH?)	→	**SET4CIP** Temperature interpolation scripts on top of SM+NETGEN (GMESH?)	→	**SET4CIP** Thermo-mechanical simulation scripts on top of Code_Aster (CA)	→	**SET4CIP** Mechanical stress distribution
IFRO(UTCN)-> UTCN		UTCN		↑		UTCN		UTCN

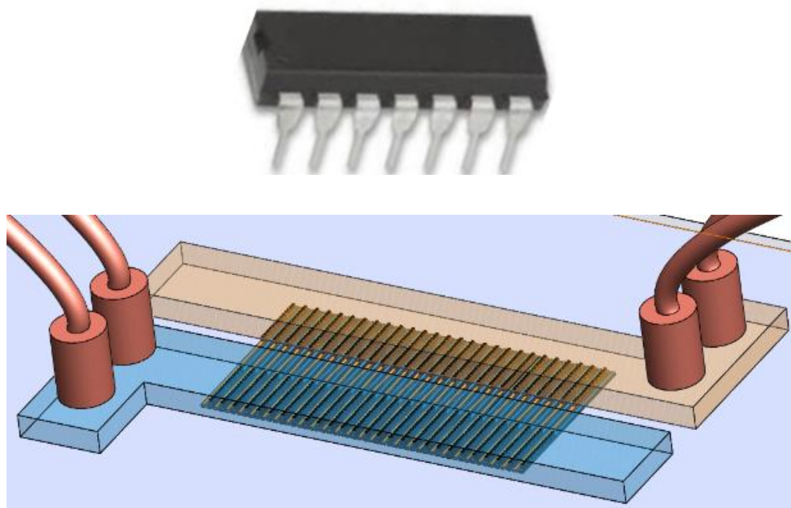
Temperature distribution
SM+Electrothermal simulator

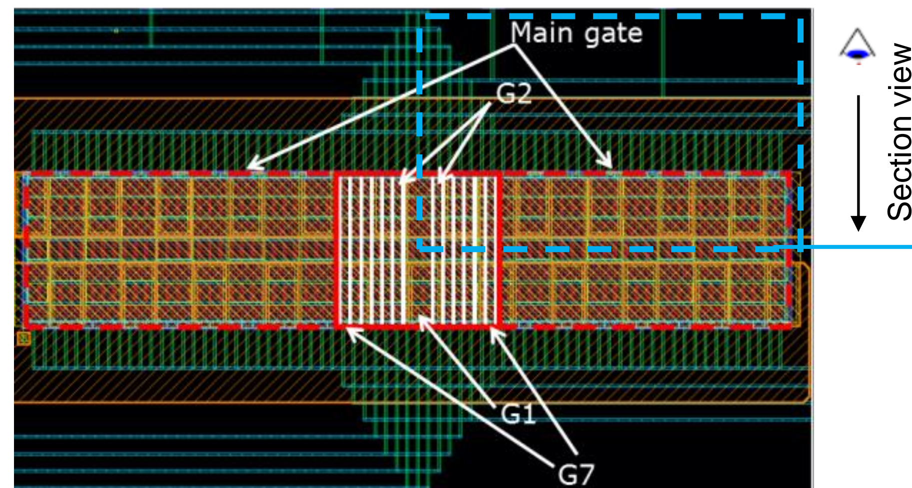
IFRO(UTCN)->UTCN

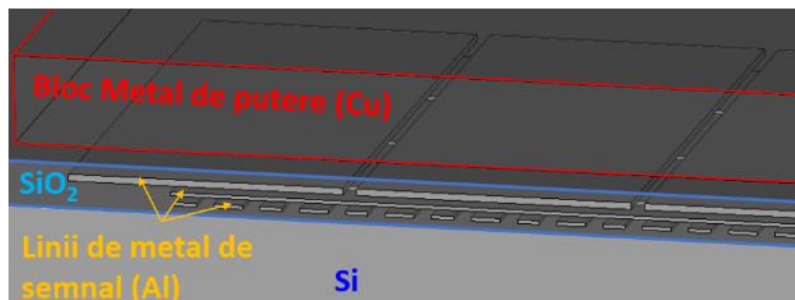
Electro-thermal simulation results

infineon

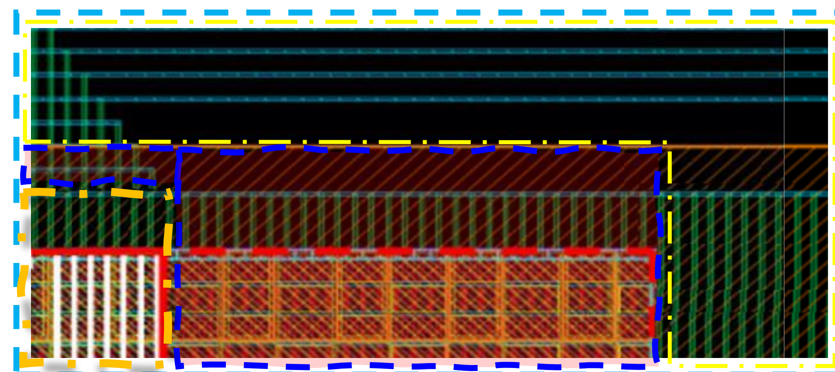




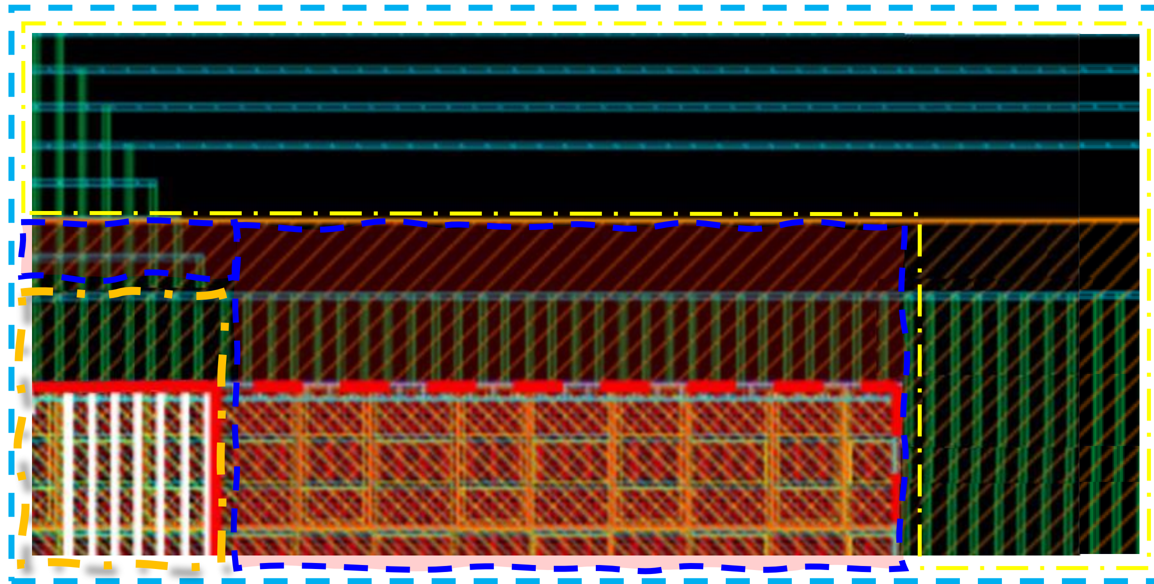




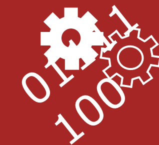
Cross section



Computational Model Definition and Model Partition



Computational Model Definition and Model Partition



Power Metal

SiO_2

Signal metal

Via

Si

Homogenized domain with equivalent properties

$c_{v_e}, \lambda_e,$
$\alpha_{CTE_e},$
E_e, ν_e

Homogenized zone

Detailed zone

M2

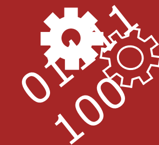
M1

SiO_2

Vias

Si

Computational Model Definition and Model Partition



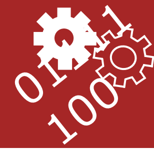
- From large-scale simplified computational model to the micro-scale high detailed computational model

1. Macro scale

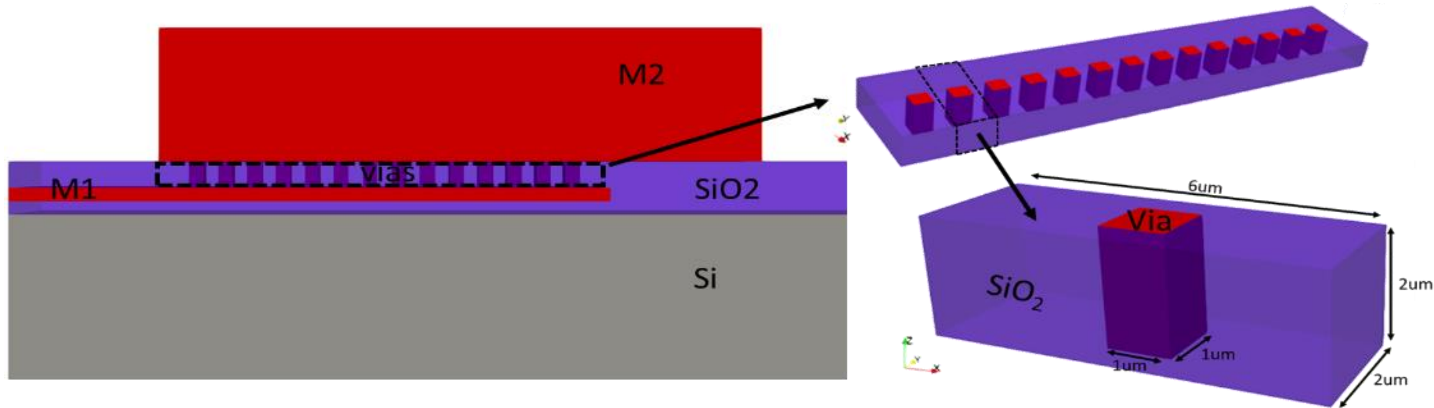
2. Meso scale (homogenized)

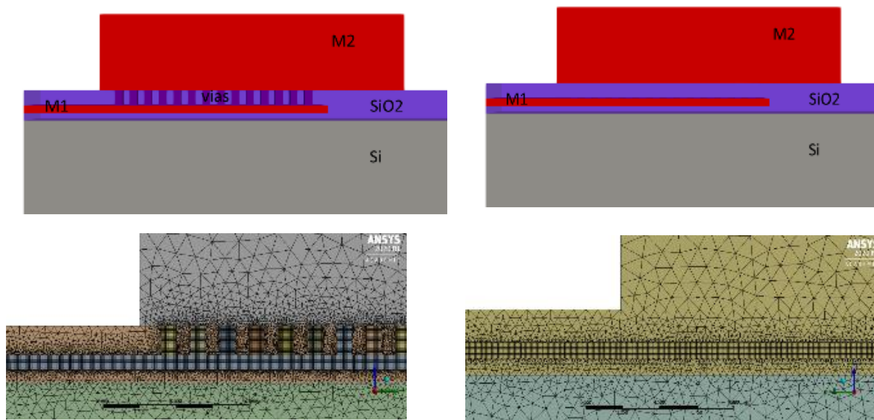
3. Micro scale

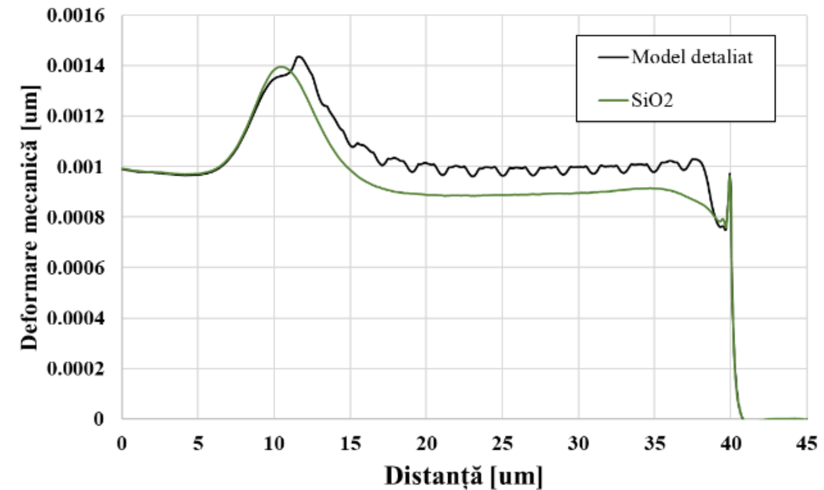
Domain Homogenization Using Equivalent Properties



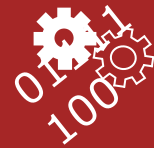
- Extraction of equivalent thermal properties
- Extraction of equivalent mechanical properties

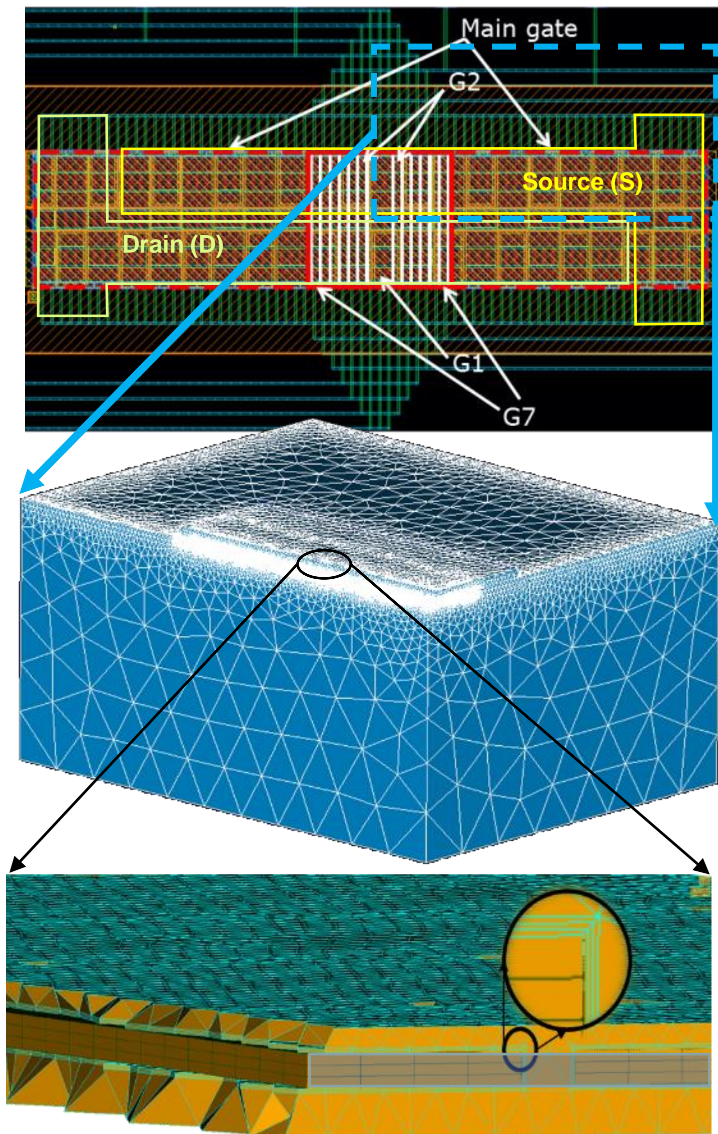


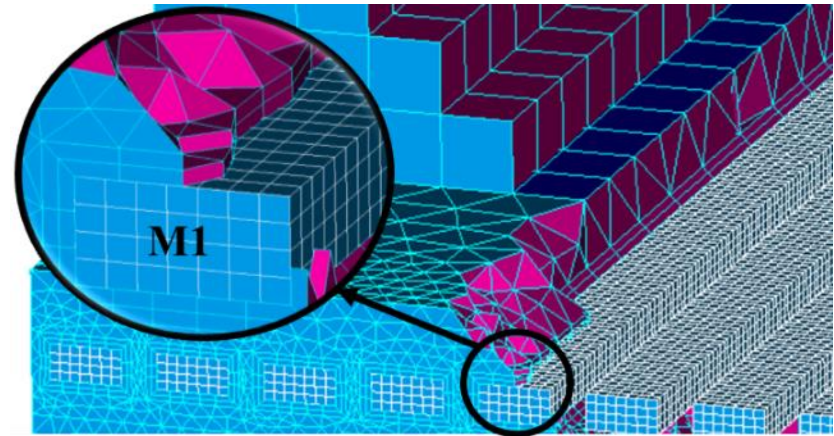


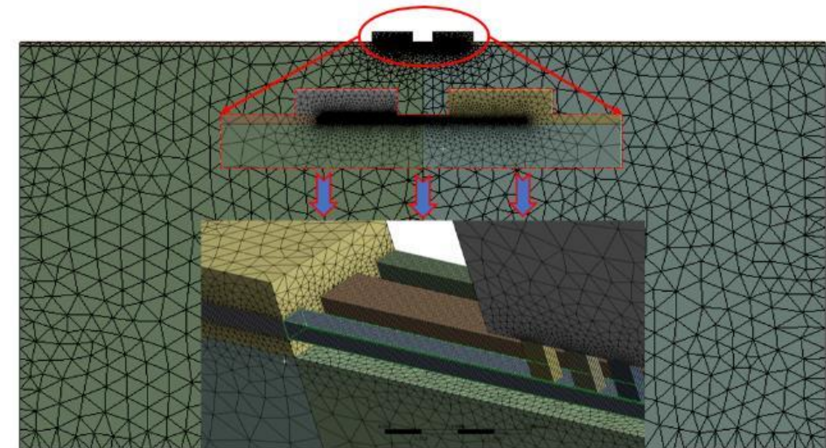


Mesh Generation on Partitioned Computational Domain



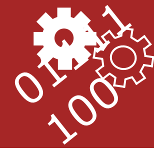


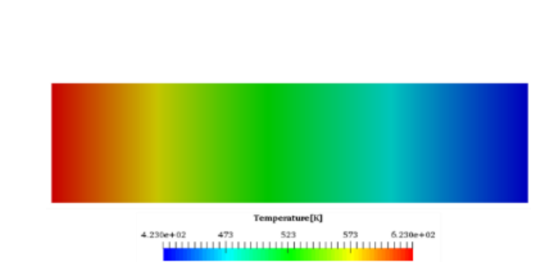


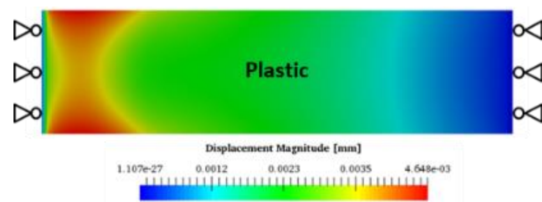


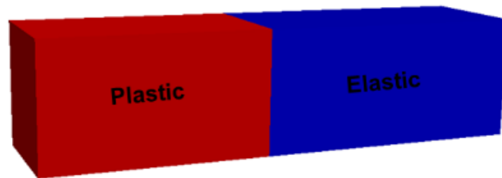
- Non partitioned domain 10.759.770 nodes
- Partitioned domain nonconformal mesh 3.473.688 nodes

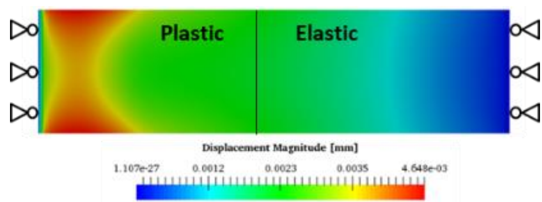
Plastic or Elastic Material Selection Based on Temperature Distribution

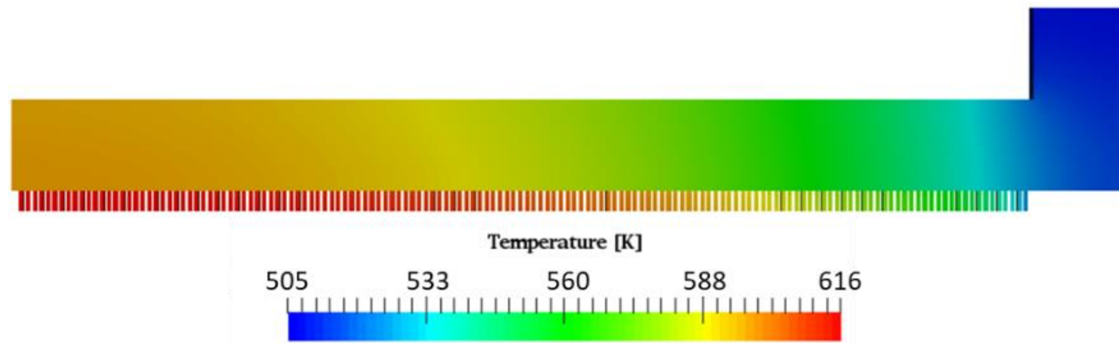


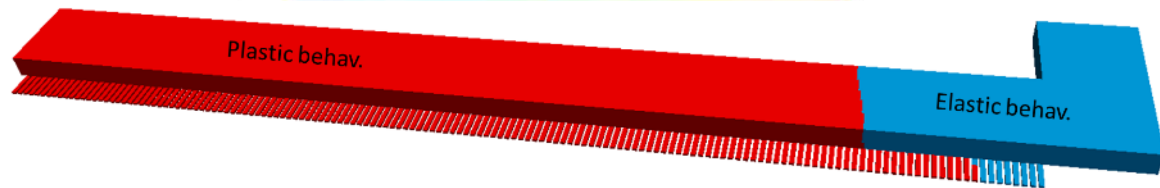


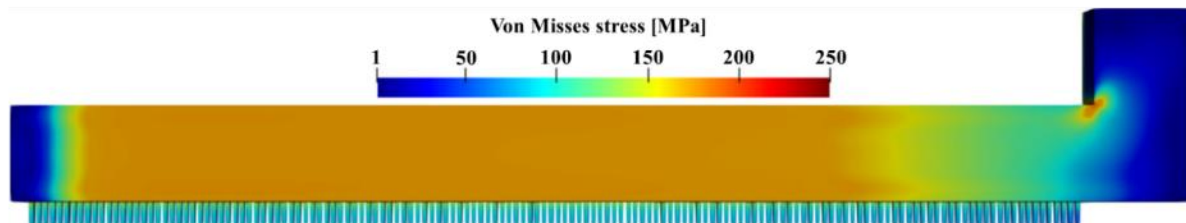


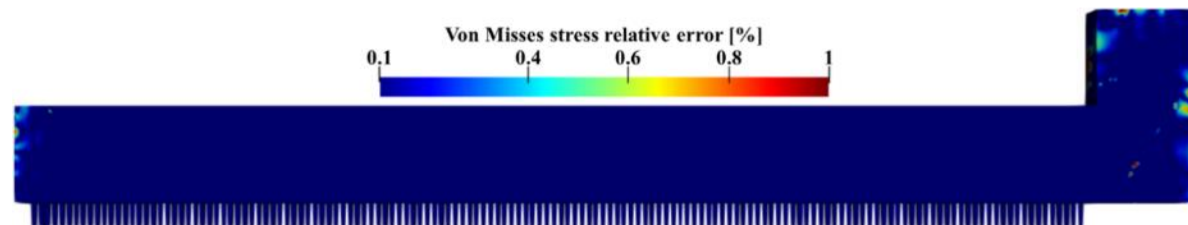




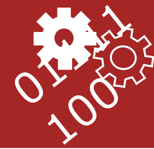


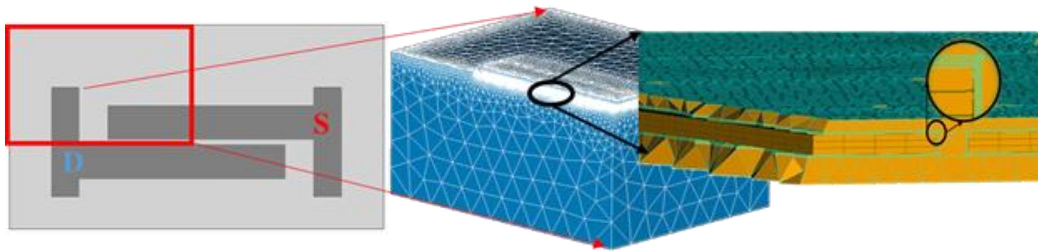


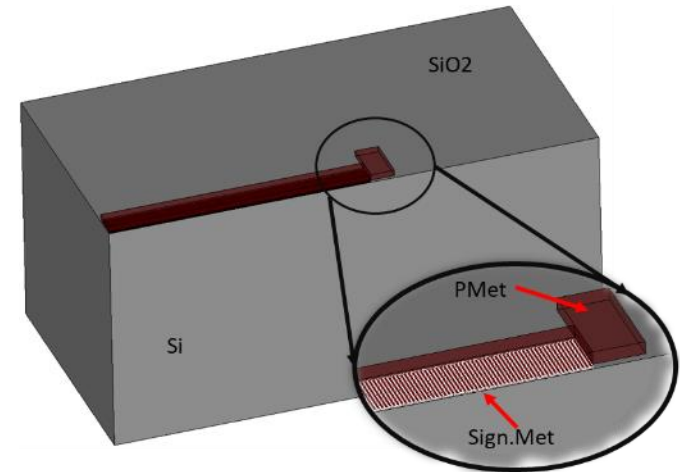


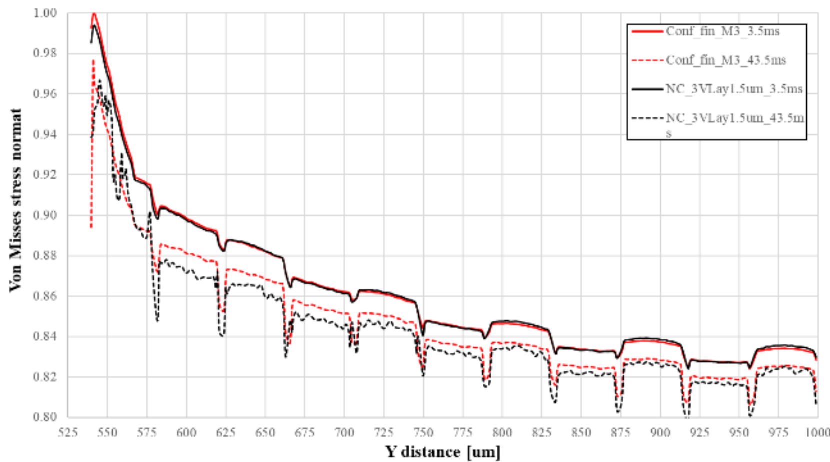


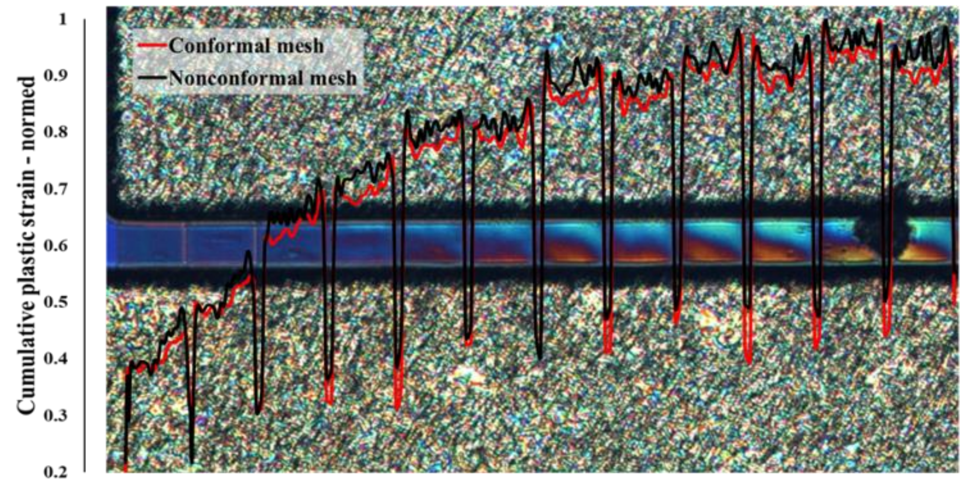
Validation of Thermo-mechanical Simulation Flow



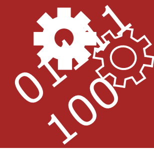








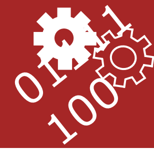
Validation of Thermo-mechanical Simulation Flow



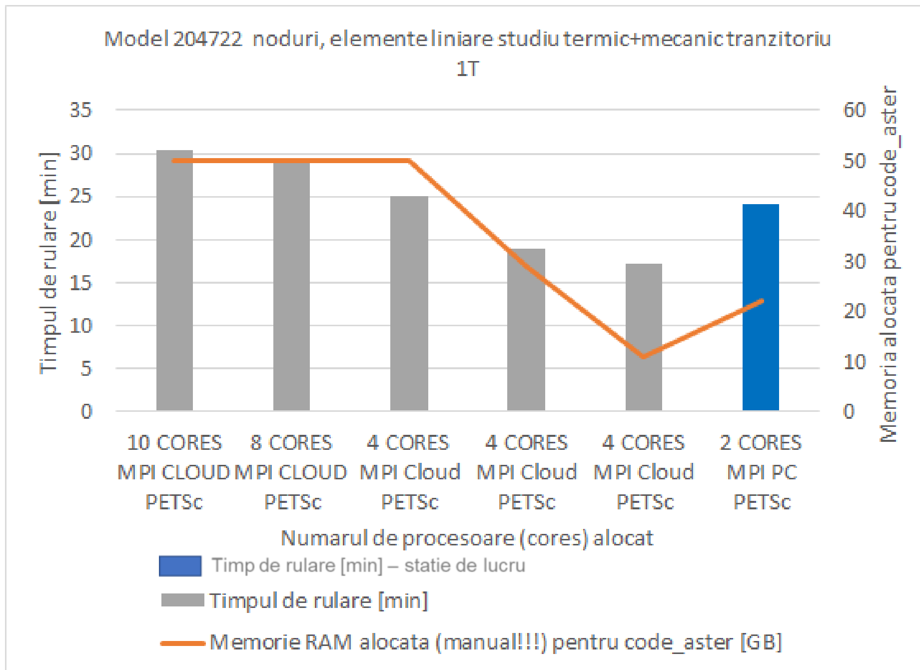
- 4 processors, c.a. 6 hours, c.a. 3 mil DOF

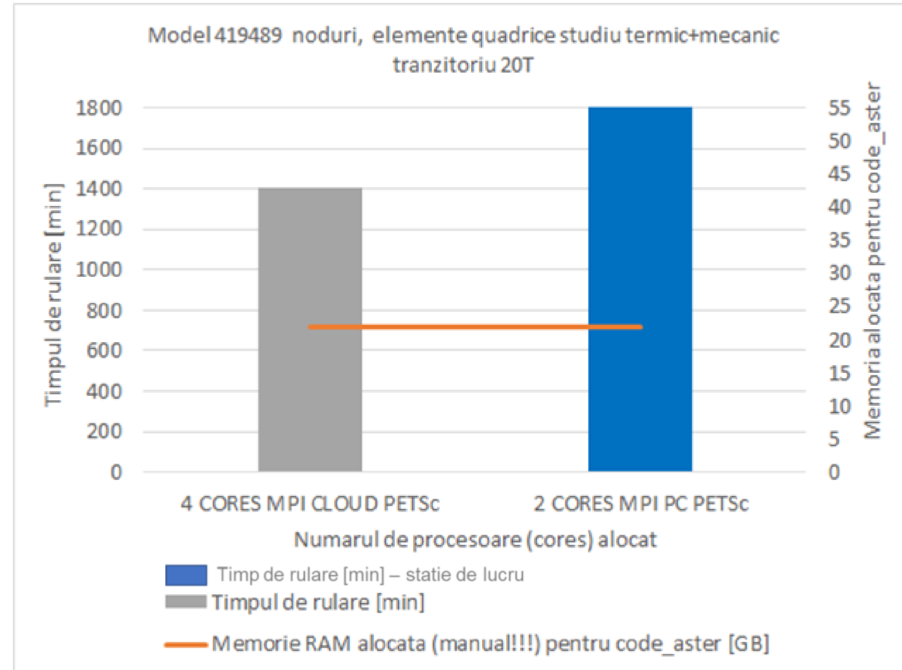
stressed oxide
Drain
Source
preparations
oxide crack
void
metal lines
metal extrusion
0 0.006 0.01 0.015 0.02

Oportunities



- Cloud computations
- Tests on the old UTCN cloud vs 1 single CPU workstation





Thank you